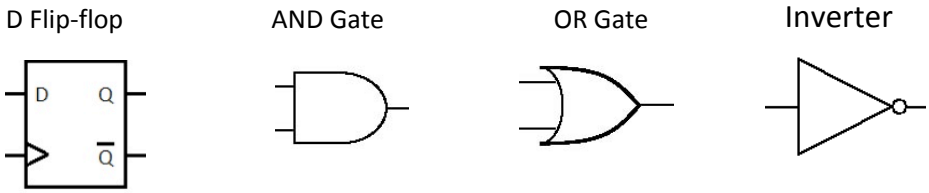
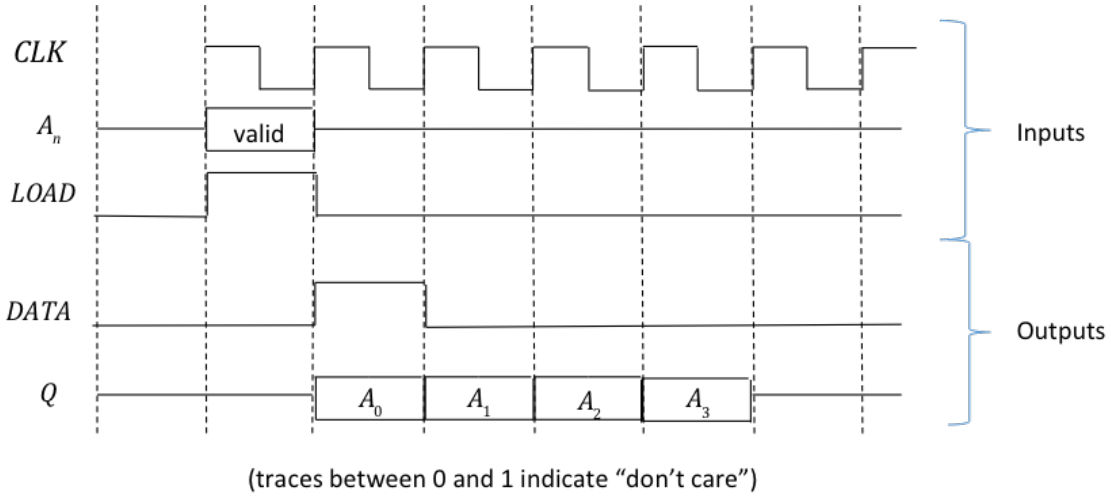
P116B Homework 2

Due 2/15/2019

1. Using the following components:



design a 4-bit synchronous "parallel to serial" converter; that is, a circuit that will load a four bit word (A_3, A_2, A_1, A_0) in response to a "LOAD" signal, and then clock the bits out serially to Q over the next four clock cycles. The circuit should also issue a DATA output concurrent with the first serial data bit, to signal the start of serial data, as illustrated in the timeline below



(traces between 0 and 1 indicate "don't care")

You may assume that the A_n bits are valid for at least one cycle, and the LOAD bit is synchronously asserted for exactly one clock cycle. There's more than one way to do this. Try to design your circuit as efficiently as possible.

(Hint: start with a shift register, and then think about how you would modify it to load in the A_n bits on a LOAD cycle, rather then the next higher bit.)

2. I want to design a bipolar DAC to operate between -5V and +5V.

   (a) If I want the LSB to be equal to or less than 1mV, what's the least number of bits I need to use?

   (b) Assuming this DAC uses "offset binary" for the input, what value would give me an output of -1V?

   (c) Answer question (b) if the DAC uses 2s complement input, with the number of bits you found in part (a).

3. Show that if the distribution of analog inputs into an ADC is broad enough that it can be considered more or less uniform over a range larger than the LSB, the RMS error on the readout due to finite quantization is given by

$$\sigma = \frac{V_{LSB}}{\sqrt{12}}$$

where V_{LSB} is the voltage change corresponding to a change of 1 on the LSB. (Hint: think about what the distribution of the difference between the true value and the digitized value looks like).

4. Based on your answer to the previous question, what's the least number of bits I need for an ADC to have a 1mV RMS error over a range of 0 to 5V due to quantization, assuming there are no other sources of noise?